In the Claims:

1. (Currently Amended) A method of assembling and testing an electronic device, comprising the steps of:

(a) fabricating a CPU on a first chip;

(b) fabricating at least one memory on a respective second chip, all said chips being physically independent;

(c) packaging said CPU with said at least one memory within a common package, with said CPU operationally connected to every said memory;

(d) testing **[[the]]** said at least one memory, using the CPU; **[[and]]**

(e) testing **[[the]]** said CPU; and

(f) storing results of said testing of said at least one memory in one of said at least one memory, by said CPU.

2. (Currently Amended) The method of claim 1, wherein said testing of **[[the]]** said CPU is effected subsequent to said testing of **[[the]]** said at least one memory.

3. (Currently Amended) The method of claim 1, further comprising the step of:

(f) loading a testing program into one of said at least one memory, **[[the]]** said CPU then testing at least one of said at least one memory by executing said testing program.

4. (Canceled)

5. (Currently Amended) The method of claim **[[4]]**1, wherein said testing of **[[the]]** said CPU includes reading said stored results from said one of said at least one memory.

6. (Original) The method of claim 1, wherein said testing of said at least one memory is effected during a burn-in of the electronic device.

7. (Currently Amended) A method of assembling and testing an electronic device, comprising the steps of:

(a) fabricating a CPU on a first chip;

(b) fabricating a nonvolatile memory on a second chip that is physically independent of said first chip;

(c) fabricating a volatile memory on a third chip that is physically independent of said first chip and said second chip;

(d) packaging said CPU and said memories within a common package with said CPU operationally connected to both said memories;

(e) loading a testing program into said volatile memory;

(**[[e]]**f) testing at least one of **[[the]]** said memories**[[,]]** by using **[[the]]** said CPU to execute said testing program; **[[and]]**

(**[[f]]**g) testing **[[the]]** said CPU.

8. (Currently Amended) The method of claim 7, wherein said testing of **[[the]]** said CPU is effected subsequent to said testing of said at least one memory.

9. (Canceled)

10. (Currently Amended) The method of claim **[[9]]**7, further comprising the step of:

(h) storing said testing program in **[[the]]** said nonvolatile memory, so that said loading of **[[the]]** said testing program into **[[the]]** said volatile memory is from **[[the]]** said nonvolatile memory.

11. (Currently Amended) The method of claim 10, wherein said loading of **[[the]]** said testing program from **[[the]]** said nonvolatile memory to **[[the]]** said volatile memory is effected by **[[the]]** said CPU.

12. (Currently Amended) The method of claim 7, further comprising the step of:

(g) storing results of said testing in **[[the]]** said nonvolatile memory, by **[[the]]** said CPU.

13. (Currently Amended) The method of claim 12, wherein said testing of **[[the]]** said CPU includes reading said stored results from said nonvolatile memory.

14. (Currently Amended) The method of claim 7, further comprising the step of:

(g) storing a testing program in **[[the]]** said nonvolatile memory, **[[the]]** said CPU then testing at least one of **[[the]]** said memories by executing said testing program directly in said nonvolatile memory.

15. (Currently Amended) The method of claim 14, further comprising the step of:

(h) storing results of said testing in **[[the]]** said nonvolatile memory, by **[[the]]** said CPU.

16. (Currently Amended) The method of claim 15, wherein said testing of **[[the]]** said CPU includes reading said stored results from said nonvolatile memory.

17. (Currently Amended) The method of claim 7,wherein said testing of at least one of **[[the]]** said memories is effected during a burn-in of the electronic device.

18. (Currently Amended) A method of assembling and testing a system-in-package, comprising the steps of:

(a) including a CPU in the system-in-package on a first chip;

(b) including a nonvolatile memory in the system-in-package on a second chip that is physically independent of said first chip;

(c) operationally connecting said CPU to said nonvolatile memory;

(d) storing, ~~a testing program~~ in **[[the]]** said nonvolatile memory, a program for testing said nonvolatile memory by steps including writing to said nonvolatile memory; and

(e) executing said ~~testing~~ program, by said CPU, in order to test **[[the]]** said nonvolatile memory.

19. (Currently Amended) The method of claim 18, further comprising the step of:

(f) loading said ~~testing~~ program from **[[the]]** said nonvolatile memory into a volatile memory, said executing of said ~~testing~~ program then being from said volatile memory.

20. (Original) The method of claim 19, further comprising the step of:

(g) including said volatile memory in the system-in-package.

21. (Currently Amended) The method of claim 18, further comprising the step of:

(f) storing results of said executing in **[[the]]** said nonvolatile memory.

22. (Original) The method of claim 18, wherein said executing is effected during a burn-in of the nonvolatile memory.

23. (Original) An electronic device comprising:

(a) a nonvolatile memory, fabricated on a first chip, wherein is stored a first testing program for testing said nonvolatile memory;

(b) a volatile memory, fabricated on a second chip and operationally connected to said nonvolatile memory, said first and second chips being physically independent prior to said operational connecting of said volatile memory to said nonvolatile memory; and

(c) a CPU, fabricated on a third chip and operationally connected to at least one of said nonvolatile memory and said volatile memory, said first, second and third chips being physically independent prior to said operational connecting of said CPU to at least one of said memories;

wherein said CPU and said memories are packaged together in a common package and wherein a second program, for testing said volatile memory, is stored in said nonvolatile memory.

24-25. (Canceled)

26. (Currently Amended) A method of assembling and testing a system-in-package, comprising the steps of:

(a) fabricating a nonvolatile memory on a first chip;

(b) fabricating a volatile memory on a second chip that is physically independent of said first chip;

(c) fabricating a CPU on a third chip that is physically independent of said first and second chips;

([[c]]d) packaging said nonvolatile memory, **[[and]]** said volatile memory and said CPU together in a common package with said nonvolatile memory, ~~operationally connected to~~ said volatile memory and said CPU operationally connected to each other;

([[d]]e) ~~executing a first testing program in order to~~ testing **[[the]]** said volatile memory by using the CPU to execute a first testing program; and

([[e]]f) storing results of said executing in **[[the]]** said nonvolatile memory.

27. (Currently Amended) The method of claim 26, further comprising the steps of:

([[f]]g) executing a second testing program in order to test **[[the]]** said nonvolatile memory; and

([[g]]h)storing results of said executing of said second testing program in [[the]] said nonvolatile memory.

28. (Original) The method of claim 26, wherein said executing is effected during a burn-in of the volatile memory.

29. (New) A method of assembling and testing an electronic device, comprising the steps of:

(a) fabricating a CPU on a first chip;

(b) fabricating a nonvolatile memory on a second chip that is physically independent of said first chip;

(c) fabricating a volatile memory on a third chip that is physically independent of said first chip and said second chip;

(d) packaging said CPU and said memories within a common package with said CPU operationally connected to both said memories;

(e) testing at least one of said memories, using said CPU;

(f) testing said CPU; and

(g) storing results of said testing in said nonvolatile memory, by said CPU.

30. (New) A method of assembling and testing an electronic device, comprising the steps of:

(a) fabricating a CPU on a first chip;

(b) fabricating a volatile memory on a second chip;

(c) packaging said CPU with said volatile memory within a common package, with said CPU operationally connected to said volatile memory;

(d) loading a testing program into said volatile memory;

(e) testing said volatile memory by using said CPU to execute said testing program; and

(f) testing said CPU.

31. (New) A method of assembling and testing an electronic device, comprising the steps of:

(a) fabricating a CPU on a first chip;

(b) fabricating at least one memory on a respective second chip, all said chips being physically independent;

(c) packaging said CPU with said at least one memory within a common package, with said CPU operationally connected to every said memory;

(d) testing said at least one memory, using the CPU; and

(f) storing results of said testing of said at least one memory in one of said at least one memory, by said CPU.

32. (New) A method of assembling and testing an electronic device, comprising the steps of:

(a) fabricating a CPU on a first chip;

(b) fabricating a nonvolatile memory on a second chip that is physically independent of said first chip;

(c) fabricating a volatile memory on a third chip that is physically independent of said first chip and said second chip;

(d) packaging said CPU and said memories within a common package with said CPU operationally connected to both said memories;

(e) loading a testing program into said volatile memory; and

(f) testing at least one of said memories by using said CPU to execute said testing program.